

What is claimed is:

- 1 1. An apparatus, comprising:
2 a first circuitry to permit access, responsive to entering a first password, to a
3 first set of resources to debug a first set of code in a memory;
4 a storage structure to contain a second password; and
5 a second circuitry coupled to the first circuitry and to the storage structure to
6 permit access, responsive to entering the second password, to a second set of resources
7 to debug a second set of code in the memory.

- 1 2. The apparatus of claim 1, wherein said access to the second set of resources is
2 through a debug interface.

- 1 3. The apparatus of claim 2, adapted to place the second set of code in a
2 substantially different portion of the memory than the first set of code.

- 1 4. The apparatus of claim 1, wherein the storage structure comprises a content
2 addressable memory.

- 1 5. The apparatus of claim 1, further comprising circuitry to prevent the access
2 responsive to said entering the first password if the access responsive to said entering
3 the second password is enabled, and to prevent the access responsive to said entering
4 the second password if the access responsive to said entering the first password is
5 enabled .

1 6. The apparatus of claim 1, wherein the storage structure comprises a programmable
2 storage structure.

1 7. The apparatus of claim 1, wherein said first set of resources comprises a first
2 portion of the memory and said second set of resources comprises a second portion of the
3 memory different than the first portion.

1 8. The apparatus of claim 1, wherein the second set of resources is substantially a
2 subset of the first set of resources.

1 9. A system, comprising:
2 a volatile first memory;
3 a second memory coupled to the first memory to contain code for execution;
4 a processor coupled to the second memory to execute the code;
5 a first storage structure coupled to the processor to contain a first password;
6 a second storage structure coupled to the processor to contain a second password;
7 and
8 circuitry to permit access, responsive to entering the first password, to a first set of
9 resources to debug a first set of code in the second memory, to disable said access to the
10 first set of resources, and to enable access, responsive to entering the second password, to a
11 second set of resources to debug a second set of code in the second memory.

1 10. The system of claim 9, wherein the first and second access are to be through a
2 debug interface.

1 11. The system of claim 9, wherein the second storage structure is a content
2 addressable memory.

1 12. The system of claim 9, wherein the circuitry is adapted to cause the access
2 responsive to said entering the first password and the access responsive to said entering the
3 second password to be mutually exclusive.

1 13. A method, comprising:
2 disabling a first password that enables performing a first set of code debug
3 operations;
4 storing a second password; and
5 entering the second password to enable performing a second set of code debug
6 operations;
7 wherein being enabled to perform the first set of code debug operations and being
8 enabled to perform the second set of code debug operations are mutually
9 exclusive.

1 14. The method of claim 13, wherein said being enabled to perform the second set of
2 code debug operations comprises being enabled to perform a subset of the first code debug
3 operations.

1 15. The method of claim 13, wherein said first and second code debug operations are
2 performed through a debug interface.

3 16. The method of claim 13, wherein said disabling the first password results from said
4 storing the second password.

1 17. The method of claim 13, further comprising enabling a third password that re-
2 enables said performing the first set of code debug operations.

1 18. A machine-readable medium that provides instructions, which when executed by a
2 computing platform, cause said computing platform to perform operations comprising:
3 receiving a first password to enable debug of a first set of code during a first debug
4 stage;
5 disabling the first password to prevent further debugging activities during the first
6 debug stage;
7 storing a second password; and
8 receiving the second password to enable debug of a second set of code during a
9 second debug stage.

1 19. The medium of claim 18, wherein the operation of disabling the first password
2 prevents access to the first set of code during the second debug stage.

1 20. The medium of claim 18, wherein the operation of storing the second password
2 results in said disabling the first password.

1 21. The medium of claim 18, wherein said operations further comprise using a third
2 password to re-enable the debug of the first set of code.

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1 22. An apparatus, comprising:
2 a processor to execute instructions in a debug mode;
3 circuitry to contain control bits; and
4 circuitry coupled to the processor and to the first circuitry to determine a level of
5 debug access permitted in the apparatus based on a state of the control bits.

1 23. The apparatus of claim 22, wherein said circuitry to contain control bits comprises
2 a set of programmable fuses.

1 24. The apparatus of claim 22, further comprising an interface coupled to the processor
2 to provide said debug access.

1 25. The apparatus of claim 22, wherein said circuitry to determine a level of debug
2 access is to determine restrictions for at least one of:
3 an address range within which said at least one instruction may be located;
4 which instructions may be executed; and
5 resources which may be accessed resultant to said execution.

1 26. The apparatus of claim 25, further comprising circuitry to abort the debug access
2 resultant to said debug access violating at least one of said restrictions.

1 27. A system, comprising:
2 a processor to execute instructions in a debug mode;
3 a volatile memory coupled to the processor;
4 circuitry to contain a set of control bits to indicate a level of debug access permitted
5 during the debug mode based on a state of at least one of the control bits; and
6 circuitry to determine if the execution violates restrictions defined by the level of
7 debug access.

1 28. The system of claim 27, wherein the state of the control bits is non-alterable after
2 manufacture of the circuitry.

1 29. The system of claim 27, further comprising circuitry to present a result of the
2 execution to a debug interface if the execution does not violate the restrictions and to not
3 present the result of the execution to the debug interface if the execution violates the
4 restrictions.

1 30. The system of claim 29, wherein the circuitry to present the result comprises
2 circuitry to abort the debug mode if the execution violates the restrictions.

1 31. The system of claim 27, wherein the circuitry to determine if the execution violates
2 the restrictions is adapted to make said determination after execution of a predetermined
3 group of at least one instruction.

1 32. A method, comprising:
2 determining, based on a set of control bits, a current level of authorized debug
3 access;
4 executing at least one instruction in a trusted subsystem in a debug mode of
5 operation; and
6 not presenting a result of said executing if said executing violates restrictions
7 defined by the current level of authorized debug access.

1 33. The method of claim 32, wherein said not presenting comprises aborting the debug
2 mode of operation.

1 34. The method of claim 32, further comprising presenting the result of said executing
2 if said executing does not violate the restrictions defined by the current level of debug
3 access.

1 35. The method of claim 32, wherein the restrictions are based on at least one of:
2 an address of the at least one instruction being within a particular memory
3 address range;

4 the at least one instruction being within a predetermined list of instructions;
5 and
6 all resources accessed by said executing being within a predetermined list of
7 resources.

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